WE CLAIM:

1. A method of encoding a product code having a first dimension systematic block code of length n_x elements and a second dimension systematic block code of length n_y elements including the steps of:

(a) applying a data element stream to first dimension encoder means to produce said first dimension systematic block code having k_x data elements and n_x-k_x parity elements, where said parity elements are derived from said k_x data elements,

(b) repeatedly applying said data element stream to said first dimension encoder means to produce k_y first dimension code vectors, where k_y is the data element length of the second dimension systematic block code,

(c) as each one of said k_y first dimension code vectors is produced, outputting said first dimension code vectors to second dimension encoder means representative of n_x encoders,

(d) deriving (n_xn_y-n_xk_y) parity elements for said second dimension systematic block code vectors, and

(e) outputting second dimension code vectors as each is produced so as to provide said encoded product code.

2. A method as claimed in claim 1, wherein said product code is a turbo product code.

3. A method as claimed in claim 1, wherein said second dimension encoder means comprises n_x encoders each

producing a total of n_y second dimension encoded elements from k_y input data elements or first dimension parity elements.

4. A method as claimed in claim 3, wherein said first dimension systematic block code is applied in sequence to said second dimension encoder means and said second dimension encoder means includes a parity generator having a random access memory (RAM) associated therewith thereby repeatedly clocking data and parity elements in to and out of said RAM to synthesize said n_x encoders.

5. A method as claimed in claim 1, wherein said systematic block code is a Hamming code.

6. A method as claimed in any of claim 1, wherein said systematic block code is an extended Hamming code.

7. A method as claimed in claim 5, wherein said data element is a single binary bit.

8. A method as claimed in claim 1, wherein said data element has a length of two or more binary digits.

9. A method as claimed in claim 1, wherein said first dimension encoder means includes a Hamming parity generator provided to produce said parity elements of said first dimension systematic block code.

10. A method as claimed in claim 9, wherein said first dimension encoder means also includes an extended Hamming parity generator adapted to receive output from said Hamming parity generator so as to produce an extended

Hamming parity element for said first dimension systematic block code.

11. A method as claimed in claim, wherein said second dimension encoder means includes a further Hamming parity generator connected to receive output from said extended Hamming parity generator so as to produce said parity elements of said second dimension systematic block code and, preferably, said second dimension encoder means also includes a further extended Hamming parity generator adapted to receive output from said further Hamming parity generator so as to produce said encoded product code.

12. A method as claimed in claim 11, wherein said second dimension encoder means also includes a further extended Hamming parity generator adapted to receive output from said further Hamming parity generator so as to produce said encoded product code.

13. A method as claimed in claim 1, wherein the output counter value of a first dimension counter having a range 0 to n_x-1 is applied to control signal generator means which supplies a clocking signal to a second dimension counter having a range 0 to n_y-1, and said control signal generator means applies control signals to said first and second dimension encoder means according to the output values of both of the aforesaid counters.

14. An apparatus for producing a product code having a first dimension systematic block code of length n_x elements and a second dimension systematic block code of length n_y elements, said apparatus including first dimension encoder means for receiving a data element stream to produce

therefrom said first dimension systematic block code having k_x data elements and n_x-k_x parity elements, where said parity elements are derived from said k_x data elements, said first dimension encoder means being arranged to produce k_y first dimension code vectors, where k_y is the data element length of the second dimension systematic block code, and second dimension encoder means representative of n_x encoders, said second dimension encoder means being arranged to receive said first dimension code vectors as they are produced and deriving (n_xn_y-n_xk_y) parity elements for said second dimension systematic block code, whereby said second encoder means is arranged to output second dimension code vectors as each is produced so as to produce said encoded product code.

15. An apparatus as claimed in claim 14, wherein said product code is a turbo product code.

16. An apparatus as claimed in claim 14 or 15, wherein said second dimension encoder means comprises n_x encoders each producing a total of n_y second dimension encoded elements from k_y input data elements or first dimension parity elements.

17. An apparatus as claimed in claim 16, wherein said second dimension encoder means includes a parity generator having a RAM associated therewith, whereby said first dimension systematic block code is applied in sequence to said parity generator and control signal generator means are provided for repeatedly clocking data and parity elements in to and out of said RAM so that n_x encoders are thereby synthesized.

18. An apparatus as claimed in claim 14, wherein said systematic block code is a Hamming code.

19. An apparatus as claimed in claim 14, wherein said systematic block code is an extended Hamming code.

20. An apparatus as claimed in claim 14, wherein said data element is a single binary digit.

21. An apparatus as claimed in claim 14, wherein said data element has a length of two or more binary digits.

22. An apparatus as claimed in claim 14, wherein said first dimension encoder means includes a Hamming parity generator provided to produce said parity elements of said first dimension systematic block code.

23. An apparatus as claimed in claim 22, wherein said first dimension encoder also includes an extended Hamming parity generator adapted to receive output from said Hamming parity generator so as to produce an extended Hamming parity element for said first dimension systematic block code.

24. An apparatus as claimed in claim 14, wherein said second dimension encoder means includes a further Hamming parity generator connected to receive output from said extended Hamming parity generator for producing said parity elements of said second dimension systematic block code.

25. An apparatus as claimed in claim 24, wherein said second dimension encoder also includes a further extended Hamming parity generator adapted to receive output from said further Hamming generator so as to produce said encoded product code.

26. An apparatus as claimed in claim 14, wherein the output counter value of a first dimension counter having a range 0 to n_x-1 is applied to control signal generator means which supplies a clocking signal to a second dimension counter having a range 0 to n_y-1, and said control signal generator means applies control signals to said first and second dimension encoder means according to the output values of both of the aforesaid counters.

27. A method of encoding a turbo product code having a first dimension systematic block code of length n_x elements and a second dimension systematic block code of length n_y elements including the steps of:

(a) applying a data element stream to first dimension encoder means to produce said first dimension systematic block code having k_x data elements and n_x-k_x parity elements, where said parity elements are derived from said k_x data elements,

(b) repeatedly applying said data element stream to said first dimension encoder means to produce k_y first dimension code vectors, where k_y is the data element length of the second dimension systematic block code,

(c) as each one of said k_y first dimension code vectors is produced, outputting said first

dimension code vectors to second dimension encoder means representative of n_x encoders, said second dimension encoder means comprising n_x encoders each producing a total of n_y second dimension encoded elements from one of k_y input data elements and first dimension parity elements,

(d) applying said first dimension systematic block code in sequence to said second dimension encoder means and said second dimension encoder means includes a parity generator having a random access memory (RAM) associated therewith thereby repeatedly clocking data and parity elements in to and out of said RAM to synthesize said n_x encoders,

(e) deriving $(n_xn_y-n_xk_y)$ parity elements for said second dimension systematic block code vectors, and

(f) outputting second dimension code vectors as each is produced so as to provide said encoded product code.

28. An apparatus for producing a turbo product code having a first dimension systematic block code of length n_x elements and a second dimension systematic block code of length n_y elements, said apparatus including first dimension encoder means for receiving a data element stream to produce therefrom said first dimension systematic block code having k_x data elements and n_x-k_x parity elements, where said parity elements are derived from said k_x data elements, said first dimension encoder means being arranged to produce k_y first dimension code vectors, where k_y is the data element length of the second dimension systematic block code, and second dimension

encoder means representative of n_x encoders, said second dimension encoder means comprising n_x encoders each producing a total of n_y second dimension encoded elements from k_y input data elements or first dimension parity elements and a parity generator having a RAM associated therewith, whereby said first dimension systematic block code is applied in sequence to said parity generator and control signal generator means are provided for repeatedly clocking data and parity elements in to and out of said RAM so that n_x encoders are thereby synthesized, said second dimension encoder means being arranged to receive said first dimension code vectors as they are produced and deriving $(n_x n_y - n_x k_y)$ parity elements for said second dimension systematic block code, whereby said second encoder means is arranged to output second dimension code vectors as each is produced so as to produce said encoded product code.